

HIGH DATA RATE DIFFERENTIAL SIGNAL LINE DESIGN FOR UNIFORM CHARACTERISTIC IMPEDANCE FOR HIGH PERFORMANCE INTEGRATED CIRCUIT PACKAGES

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BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates generally to the field of integrated circuit (IC) design. In particular, the present invention relates to differential signal line design for multi giga-hertz GHz data rates on the high performance IC packages.

Related Art

[0002] For high pin-count packages, a significant challenge lies in escaping high data rate input/output (IO) differential signals from the IC, or die, to the package. In escaping these high data rate signals, a designer will preferably provide for escaping the signals without impacting signal integrity.

[0003] Using conventional techniques, signals are escaped from the die near the die-package interface with virtually no concern for signal integrity. This approach might be suitable for relatively low frequency signals, i.e., signals having data rates below one giga-bit per second (Gbps). But as the signal data rates increase, for example, beyond about 5 Gbps, the methodology for escaping the signals from the die becomes absolutely critical.

[0004] Because of limited space on the die, the signals are traditionally routed without concern for line factors such as characteristic impedance and the cross-talk between adjacent signal lines. Unfortunately, however, these factors degrade signal quality by producing unwanted reflections due to the impedance mismatches, and signal coupling between the adjacent lines.

[0005] What is needed, therefore, is a technique for escaping high data rate differential signals while, at the same time, maintaining signal integrity. More specifically, what is needed is a technique for providing substantially uniform

impedances across all portions of the signal lines used to escape high data rate differential signals. Finally, what is needed is a technique that minimizes cross-talk between adjacent signal lines carrying the differential signals.

SUMMARY OF THE INVENTION

[0006] Consistent with the principles of the present invention as embodied and broadly described herein, an exemplary apparatus includes an integrated circuit (IC) mounted on a chip carrier. The IC has one or more differential pair circuits coupled thereto and the chip carrier has a signal escaping portion and a remaining portion. The apparatus also includes differential signal lines coupled to the differential pair circuits, the differential signal lines (i) extending through the chip carrier and (ii) having first and second segments. The first segment extends through the escaping portion and the second segment extends through the remaining portion. The first and second segments have respective first and second widths.

[0007] The present invention facilitates the design of signal lines suitable for transmitting high data-rate differential signal without inducing significant impacts to signal integrity. Signal lines that carry high data-rate differential signals are designed in a differential ended configuration. The characteristic impedance of the differential line pair, that transmits the signals, primarily depends on the line trace width, line spacing, and dielectric thickness. By properly varying the trace width and the spacing, the characteristic impedance will also vary.

[0008] In the present invention, the escape area of the differential signal line is designed to be, for example, about 100 ohms with a narrow trace width and narrow spacing between the signal lines. Particularly, the spacing between inverting and non-inverting paths of the differential signal line is selected such that the cross-talk is reduced to about 1% (-40db). Beyond the escape area, the characteristic impedance can be maintained at about 100 ohms by increasing the trace width and line spacing. An advantage of increasing the

trace width beyond the escape area is that the resistance of the line is reduced, ultimately reducing the insertion loss.

[0009] Further embodiments, features, and advantages of the present invention, as well as the structure and operation of the various embodiments of the present invention are described in detail below with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE FIGURES

[0010] The accompanying drawings, which are incorporated in and constitute part of the specification, illustrate embodiments of the invention and, together with the general description given above and the detailed description of the embodiments given below, serve to explain the principles of the present invention. In the drawings:

[0011] FIG. 1 is a top-level block diagram of an electrical circuit constructed and arranged in accordance with an embodiment of the present invention;

[0012] FIG. 2 is a more detailed view of the transmission lines shown in FIG. 1 above; and

[0013] FIG. 3 is a graphical illustration of improved insertion loss and cross-talk, as provided through use of an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0014] The following detailed description of the present invention refers to the accompanying drawings that illustrate exemplary embodiments consistent with this invention. Other embodiments are possible, and modifications may be made to the embodiments within the spirit and scope of the invention. Therefore, the detailed description is not meant to limit the invention. Rather, the scope of the invention is defined by the appended claims.

[0015] It would be apparent to one of skill in the art that the present invention, as described below, may be implemented in many different embodiments of

software, hardware, firmware, and/or the entities illustrated in the figures. Any actual software code with the specialized control of hardware to implement the present invention is not limiting of the present invention. Thus, the operational behavior of the present invention will be described with the understanding that modifications and variations of the embodiments are possible, given the level of detail presented herein.

[0016] FIG. 1 is a top-level block diagram of an electrical circuit structured and arranged in accordance with the present invention. In FIG. 1, an electrical circuit 100 includes a printed circuit board (PCB) 102 and an electronic component package 103, or chip carrier, mounted on the PCB 102. A die 106 is electrically coupled to the package 103.

[0017] Differential circuit components 108 and 109 are formed within the die 106. The differential circuit components 108 and 109 could be, for example, differential drivers such as amplifiers. A signal transmission line 110 connects the differential circuit component 109 to the PCB 102, and in turn, to another package 104, also mounted on the PCB 102. The transmission line 110 further connects the package 104 to an additional die 105. The signal line 110 extends through an initial portion of the package 103 and then through a signal via 114 (remaining portion). Similarly, the transmission line 111 provides an electrical connection between the differential circuit component 108, the die 106, the package 103, the PCB 102, the package 104, and the die 105.

[0018] As known in IC design parlance, an escape area is an area within a package, such as the package 103, between the entry point of an electrical signal and the point at which the signal enters the signal via. In the present invention, as illustrated in FIG. 1, a portion 112 is the signal escape area. A portion 113 denotes the remaining portion within the package 103, wherein the signal line 110 is routed through the via 114 and then exited from the package 103. FIG. 2 provides a more detailed illustration of the die 106 and the associated signal lines 110 and 111 shown in FIG. 1.

[0019] As illustrated in FIG. 2 and noted above, the signal lines 110 and 111 share identical characteristics. Therefore, the techniques and features

discussed with reference to the signal lines 110 are also applicable to the signal lines 111. The signal line 110 is shown in a differential-ended configuration having an inverting pathway 200 and a non-inverting pathway 202. Additionally, the line 110 includes a first segment 204, and a second segment 210. The inverting pathway 200 and the non-inverting pathway 202 are also respectively known as the negative and positive signal line sides.

[0020] The first segment 204 has a first length 206 and a first width 208. The second segment 210 has a second length 212 and a second width 214. Exemplary widths can include values within a range of about 25 – 100 microns (μm). The inverting path 200 and the non-inverting path 202 are adjacent to one another and are separated by a first spacing 216 and a second spacing 218, as shown in FIG. 2. Exemplary spacings can include values within a range of about 25 – 200 μm . A transition area 220 is provided where the first segment 204 transitions into the second segment 210.

[0021] In modern IC design, spacing between components, such as the differential components 108 and 109, is typically within a range of about 30-50 μm . And spacing within this range provides very restricted areas for escaping high data-rate signals from the die 106 to the electrical package 103. Subsequently, the signal lines in the escape areas are typically required to be narrow in order to physically conform to the limited space between the components. However, escaping high data-rate signals using narrow signal lines causes the resistance of the lines to be high. Another factor that contributes to this high resistance is the signal line length.

[0022] In conventional integrated circuit design, the differential signal lines are therefore narrow and maintain the same width and spacing throughout the electrical package. As the length of these conventional signal lines increases, the resistance increases, thus degrading the signal quality.

[0023] In the present invention, however, the signal lines 110 include at least the first segment 204 and the second segment 210, having different trace widths and different spacings. The segment 204 is narrow and escapes high data-rate differential signals from the escape area 112 of the package 113. The

other segment 210 is wider and facilitates transmission of the signal through the remaining portion 113 of the package 103. Providing these multiple segments having varying widths and spaces provides a substantially uniform impedance across the entire length of the signal line 110 as it traverses the electrical package 103.

[0024] Precise values for widths 208 and 214 can be determined based upon the use of standard commercial turn-key modeling and simulation tools. Factoring in the dielectric properties of the segment 204 within the escape area 112, the characteristic impedance can be modeled to a variety of exemplary values, such as 100 ohms. As noted in FIG. 2, as the signal line 110 exits the escape area 112 and enters into the via 113, the dielectric width 214 and the spacing 218 are increased.

[0025] As the dielectric width 214 increases, the resistance in the segment 210 correspondingly decreases, subsequently reducing the insertion loss. By varying the widths 208 and 214 in this manner, a substantially uniform characteristic impedance can be achieved across these segments. In the present invention, the lengths 206 and 212 can also be determined through use of the turn-key modeling and simulation tools noted above.

[0026] In similar fashion, cross-talk between the inverting and non-inverting paths 200 and 202 respectively, can be reduced by varying the path spacing 218 from the spacing 216 within the areas 112 and 113. Here again, standard off-the-shelf modeling and simulation tools can precisely determine the values of the spacings 216 and 218 as well as other line dimensions in order to maintain uniform impedance across the line 110. By varying these spacings, the cross-talk between the inverting and the non-inverting paths can be substantially reduced. FIG. 3 graphically illustrates the insertion loss and cross-talk achieved through implementation of an embodiment of the present invention.

[0027] FIG. 3 provides a graphic illustration 300 conveying frequency values 302 and amplitude values 304 of reductions in insertion loss 306 and cross-talk 308 provided by the present invention. In particular, FIG. 3 shows that as

the data rates of the differential signal increases, the insertion loss for differential pairs realizes an improvement of 5-6 dB over the conventional techniques. In the example of FIG. 3, the improvement is illustrated as being most significant, for example, at about 30 GHz. FIG. 3 also conveys that the cross-talk between adjacent lines can be reduced to about - 40 dB, providing about a 15-20 dB improvement in cross-talk over conventional techniques.

[0028] In the present invention, the signal lines through the package are designed to improve the overall integrity of high data-rate differential signals passed therethrough. This approach provides substantially uniform impedance throughout the length of the package, reducing insertion losses. The technique of the present invention also improves the impedance match to the drivers and the PCB traces, reduces cross-talk between the differential signal lines, and supports high-data rate signals with reduced jitter.

[0029] The present invention has been described above with the aid of functional building blocks illustrating the performance of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0030] Any such alternate boundaries are thus within the scope and spirit of the claimed invention. One skilled in the art will recognize that these functional building blocks can be implemented by analog and/or digital circuits, discrete components, application specific integrated circuits, firmware, processors executing appropriate software and the like or any combination thereof. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.